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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,864	01/10/2001	Yoshinori Tanaka	49657-904	6644

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/756,864	TANAKA ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-16 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/095,612* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The final rejection mailed 12/14/01 was defective in that new art (Gonzalez et al. 5,208,180) was cited that was not of record. The final rejection dated 12/14/01 is therefore withdrawn and replaced by the present action.

2. The amendment filed on 09/27/01 has been entered.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/095,612, filed on 06/11/1998.

The amendment found in item 9 of Applicant's 1/10/01 Request Form has been entered. Applicant must further amend the first line of his application to end with the text, "now Patent No. 6,194,758."

Correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over GONZALEZ et al. (5,168,073) in view of GONZALEZ et al. (5,208,180).

Gonzalez et al. '073 discloses a DRAM with a memory cell region and peripheral circuit region comprising a semiconductor substrate 3 having a major surface, an insulating film 75 having an upper surface 114, being formed on the semiconductor substrate 3 to extend from the memory circuit to the peripheral circuit, first and second capacitor lower electrodes 90 being adjacent to each other through the insulating film 75, being formed on the surface of the semiconductor substrate 3 and extending to a vertical position substantially identical to the upper surface of the insulating film 75 in the memory region, and a capacitor upper electrode 120 formed on the capacitor lower electrode 90 through a dielectric film 115 to extend onto the upper surface 114 of the insulating film 75. Note figures 6 and 10, and col. 5 l. 60 of Gonzalez et al.

With regard to claim 14, Gonzalez et al. '073 discloses that the insulating film includes upper insulating film 75 made of BSPG and lower insulating film 40 made of oxide, the two layers, on account of being made of different materials, being different in etching rate from each other. Note figure 10 of Gonzalez et al.

With regard to claim 15, Gonzalez et al. '073 discloses the dielectric film 115 is formed between the entire side surface of the capacitor lower electrode 90 and the insulating film 75. For this reason it is formed "at least" either a side surface or only a

part of the bottom surface of the capacitor lower electrode 90 and the insulating film 75. Note figures 10 of Gonzalez et al.

Gonzalez et al. '073 does not disclose that the upper electrode is formed on an interior region of each of the first and second lower electrodes.

However, Gonzalez et al. '180 discloses a DRAM capacitor wherein the upper electrode 58 is formed on an interior region of the lower electrode 42. Note figure 12 of Gonzalez et al. '180. Therefore, it would have been obvious to a person having skill in the art to replace the upper electrode formed on the outer surface of the lower electrodes of Gonzalez et al. '073's DRAM with the upper electrode formed on the interior region of the lower electrodes such as taught by Gonzalez et al. '180 in order to increase the available area upon which the upper electrode faces the lower electrodes to thus provide higher capacitance, more charge storage, and allow a lower refresh rate.

Claims 13, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over GONZALEZ et al. (5,168,073) in view of GONZALEZ et al. (5,208,180), as applied to claim 12 above, and further in view of WANG et al. (5,856,220).

Gonzalez et al. '073 and '180 disclose all the limitations of claims 21-23 except that the part of the insulating film between adjacent first and second electrodes have a width smaller than the minimum working size formable by photolithography. Note figure 10 of Gonzalez et al. '073, figure 12 of '180.

However, Wang et al. discloses a method whereby isotropic etching cuts through the insulating film in a pair of hemispherical cuts to produce a pair of adjacent lower electrodes. The width of the part of the insulating film this method leaves between the

adjacent electrodes is wholly independent of the limits of photolithography. The width may be zero, or any number larger than zero. Note figure 12 of Wang et al. Therefore, it would have been obvious to a person having skill in the art to reduce wasted space occupied by part of the insulating film by replacing the two dimensionally patterned, lithographically size restricted cylindrical lower electrodes of Gonzalez et al.'s device with the hemispherical, free form etched lower electrodes such as taught by Wang et al. in order to increase electrode area to thus provide higher capacitance.

Gonzalez et al. '073 and '180 disclose all the limitations of claim 13 except that a side surface of the capacitor lower electrode has a curved plane. Note figure 10 of Gonzalez et al. '073, figure 12 of '180.

However, Wang et al. discloses a method that produces a lower electrode with hemispherical, curved side planes. Note figure 12 of Wang et al. Therefore, it would have been obvious to a person having skill in the art to replace the cylindrical side planes of Gonzalez et al.'s lower electrode with the hemispherical, curved side planes such as taught by Wang et al. in order to increase electrode area to thus provide better higher capacitance.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over GONZALEZ et al. (5,168,073) in view of GONZALEZ et al. (5,208,180), as applied to claim 12 above, and further in view of NAKANO (JP 06125051).

Gonzalez et al. '073 and '180 disclose all the limitations of claim 16 except that the capacitor lower electrodes comprise granular crystals on their surfaces. Note figure 10 of Gonzalez et al. '073, figure 12 of '180.

However, Nakano discloses stack type DRAM capacitor with an undulating surface due to its granularity. Note figure 1d of Nakano. Therefore, it would have been obvious to a person having skill in the art to replace the smooth surfaced lower electrodes of Gonzalez et al.'s DRAM capacitor with lower electrodes having an undulating surface due to granularity such as taught by Nakano in order to increase effective electrode area to thus provide higher capacitance.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over GONZALEZ et al. (5,168,073) in view of GONZALEZ et al. (5,208,180), in view of WANG et al. (5,856,220), as applied to claim 21 above, and further in view of the admitted prior art.

Gonzalez et al. and Wang et al. discloses all the limitations of claim 16, including a "hard" oxide peripheral circuit element protection film 40 disclosed by Gonzalez et al., except that the capacitor upper electrode extends towards the peripheral circuit, and to provide an upper interlayer isolation film with a contact hole formed therein on the capacitor upper electrode. Note figure 10 of Gonzalez et al.'073, figure 12 of '180, and figure 12 of Wang et al.

However, the admitted prior art discloses a stack type DRAM capacitor with the upper capacitor electrode1151 extended towards the peripheral circuit, and which provides an upper interlayer isolation film 1205 disposed over the upper capacitor electrode 1151, with a contact hole 1135 formed therein on the capacitor upper electrode 1151. Note figure 117 of the admitted prior art. Therefore, it would have been obvious to a person having skill in the art to extend the upper electrode of Gonzalez et al. and Wang et al.'s DRAM capacitor towards the peripheral circuit, and to provide an

upper interlayer isolation film with a contact hole formed therein on the capacitor upper electrode, along with a peripheral circuit element protection film formed under the insulating film such as taught by the admitted prior art in order to allow electrical access to the upper capacitor electrode in the peripheral region and allow the contact hole to be made by a non-critical etch step to thus provide more efficient manufacture.

Response to Arguments

5. Applicant's arguments filed 02/16/00 have been fully considered but they are not persuasive.

It is argued, at page 6 of the remarks, that "In direct contrast to amended claim 12, the lower electrodes of Gonzalez et al. ['073] is not shaped so as to have an interior portion..."It is further argued, at page 6 of the remarks, that "[t]he structural differences the present invention and the device of Gonzalez et al. ['073] are significant and functionally meaningful." It is further argued, at page 7 of the remarks, that "the capacitor lower electrode has a so-called cup shape, allowing positioning of the upper electrode on the interior peripheral portion thereof." In view of the new grounds of rejection, these arguments are considered moot.

It is further argued, at page 8 of the remarks, that "[i]n particular, FIG. 13 of Wang et al. discloses etching the portion of the lower electrode **74** using standard photolithographic techniques in order to separate the adjacent lower electrodes (col. 8, lines 32-44)." However, since claims 13 and 21-24 are rejected in view of the disclosure in Wang et al.'s figure 12, Applicant's argument is not currently relevant.

Regarding claims 16 and 24, it is argued, at page 8 of the remarks, that "Applicant asserts, as explained above, that Gonzalez et al. do not disclose or suggest all the features recited in amended base claim 12." This argument, like the argument regarding claim 12, is moot in view of the new grounds of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 3-C23. The faxing of such papers must conform

to the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2826 Fax Center number is (703) 308-7722 and 308-7724. The Group 2800 Fax Center is to be used only for papers related to Group 2800 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to Thomas Dickey whose telephone number is **(703) 308-0980**. The Examiner is in the Office generally between the hours of 7:00 AM to 6:00 PM (Eastern Standard Time) Monday through Thursday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**.

TLD
01/2002

Minh Loan Tran
Primary Examiner